IN THE CLAIMS:

The claims are pending as follows:

1-70. (Cancelled)

71. (Previously Presented) A transistor comprising:

a spin injector for injecting spin-polarized hot carriers by a spin-filter effect; and

a spin analyzer for selecting the thus injected spin-polarized hot carriers by the spin-filter effect.

72. (Previously Presented) The transistor according to claim 71, wherein said spin injector comprises:

a first ferromagnetic barrier layer through which the carriers can be transported by tunneling upon application of a voltage across said first ferromagnetic barrier layer;

a first nonmagnetic electrode layer joined to one end surface of said first ferromagnetic barrier layer; and

a second nonmagnetic electrode layer joined to the other end surface of said first ferromagnetic barrier layer.

73. (Previously Presented) The transistor according to claim 71, wherein said spin analyzer comprises:

a second ferromagnetic barrier layer;

said second nonmagnetic electrode layer joined to one end surface of said second ferromagnetic barrier layer; and

a third nonmagnetic electrode layer joined to the other end surface of said second ferromagnetic barrier layer, wherein said second nonmagnetic electrode layer is common to said spin injector and said spin analyzer.

74. (Previously Presented) The transistor according to claim 72, wherein said first and second ferromagnetic barrier layers comprise a ferromagnetic semiconductor or a ferromagnetic insulator.

75. (Previously Presented) The transistor according to claim 72, wherein the thickness of said second nonmagnetic electrode layer is smaller than the mean free path of the spin-polarized hot carriers in said second nonmagnetic electrode layer.

76. (Previously Presented) A transistor according to claim 72, wherein the spin-filter effect of said spin injector takes advantage of the fact that, in a carrier tunneling effect in said first ferromagnetic barrier layer which is produced through the application of a voltage to said first nonmagnetic electrode layer and to said second nonmagnetic electrode layer, those of the carriers that exist in said first nonmagnetic electrode layer and that have a spin direction parallel to a spin band at the band edge of said first ferromagnetic barrier layer have a large tunneling probability, while those carriers with an antiparallel spin direction have a small tunneling probability.

77. (Previously Presented) The transistor according to claim 72, wherein the spin-filter effect of said spin analyzer takes advantage of the fact that, when the spin direction of the spin-polarized hot carriers injected from said spin injector is parallel to that of the spin band at the band edge of said second ferromagnetic barrier layer, said spin-polarized hot carriers are transported through the spin band at the band edge of said second ferromagnetic barrier layer and reach said third nonmagnetic electrode layer, whereas when the spin direction of said spin-polarized hot carriers is antiparallel to that of the spin band at the band edge of said second ferromagnetic barrier layer, said spin-polarized hot carriers are unable to reach said third nonmagnetic electrode layer.

78. (Previously Presented) The transistor according to claim 72, wherein a first voltage is applied between said first nonmagnetic electrode layer and said second nonmagnetic electrode layer from a first power supply, and a second voltage is applied between said second nonmagnetic electrode layer and said third nonmagnetic electrode layer or between said first nonmagnetic electrode layer and said third nonmagnetic electrode layer, from a second power supply, and wherein said spin-polarized hot carriers injected from said first nonmagnetic electrode layer to said second nonmagnetic electrode layer are switched to a current through said second ferromagnetic barrier layer and said second power supply or a current through said second nonmagnetic electrode layer and said first power supply depending on the relative magnetization configuration of said first ferromagnetic barrier layer and said second ferromagnetic

barrier layer.

79. (Previously Presented) The transistor according to claim 78, wherein said first voltage is applied such that the energy of the injected spin-polarized hot carriers becomes larger than the spin band edge energy at the band edge of the said second ferromagnetic barrier layer and smaller than the energy of the spin band edge to which the spin-split width is added.

80. (Previously Presented) The transistor according to claim 79, wherein the relative magnetization configuration in said first ferromagnetic barrier layer or said second ferromagnetic barrier layer can be reversed with the application of a magnetic field.

81. (Previously Presented) A memory circuit comprising a memory cell formed by the transistor according to claim 71.

82. (Previously Presented) The memory circuit according to claim 81, wherein said second nonmagnetic electrode layer of said transistor is connected to a wordline, said third nonmagnetic electrode layer of said transistor is connected to a bitline, said bitline is connected to a power supply via a load, and said first nonmagnetic electrode layer of said transistor is connected to ground.

83. (Withdrawn) A memory element comprising:

a transistor containing a ferromagnet and having output characteristics that depend on the spin direction of carriers (to be hereafter referred to as a "spin transistor");

an information writing means for writing information within said spin transistor by changing the magnetization configuration of said ferromagnet; and

an information sensing means for sensing from said output characteristics information stored in said spin transistor in terms of a magnetization configuration.

84. (Withdrawn) The memory element according to claim 83, wherein said spin transistor comprises a free layer having at least one ferromagnet in which the relative magnetization configuration can be independently controlled, and a pin layer having a ferromagnet in which the relative magnetization configuration is not changed,

wherein

one of a first memory state in which said free layer and said pin layer have the same relative magnetization configuration, and a second memory state in which they have different magnetization configurations, is retained.

85. (Withdrawn) A memory element according to claim 84, wherein a single spin transistor stores information in terms of the relative magnetization configuration of said free layer relative to said pin layer, and wherein information stored in said transistor is detected using the output characteristics of said spin transistor, which depend on the relative magnetization configuration of said pin layer and said free layer.

86. (Withdrawn) The memory element according to claim 84, wherein said spin transistor comprises: a first electrode structure for injecting spin-polarized carriers;

a second electrode structure for receiving said spin-polarized carriers; and

a third electrode structure for controlling the amount of the spin-polarized carriers transported from said first electrode structure to said second electrode structure, wherein

said pin layer and said free layer are included in any of said first to third electrode structures.

87. (Withdrawn) A memory element comprising:

a single spin transistor described in claim 86;

a first line connecting said first electrode structure to ground;

a second line connected to said second electrode structure; and

a third line connected to said third electrode structure.

88. (Withdrawn) A memory element comprising:

a single spin transistor according to claim 86;

a first line connecting said first electrode structure to ground;

a second line connected to said second electrode structure;

a third line connected to said third electrode structure;

an output terminal formed at one end of said second line; and

a fourth line branching from said second line and connected to a power supply

via a load.

89. (Withdrawn) The memory element according to claim 87, further comprising a first separate line and a second separate line that intersect one another above said spin transistor in an electrically insulated manner.

90. (Withdrawn) The memory element according to claim 89, wherein said first separate line and/or said second separate line are replaced with said second line and/or said third line.

91. (Withdrawn) The memory element according to claim 89, wherein information is written by reversing the magnetization of said free layer by a magnetic field induced by causing a current to flow through said first separate line and said second separate line, or through said second line and said third line, thereby changing the relative magnetization configuration between said pin layer and said free layer.

92. (Withdrawn) The memory element according to claim 87, wherein information is sensed using the output characteristics of said spin transistor when a first bias is applied to said third line and a second bias is applied between said first line and said second line.

93. (Withdrawn) The memory element according to claim 88, wherein information is sensed using an output voltage that is obtained on the basis of a voltage drop across said load due to a current through said load and said spin transistor between said power supply and said first line when a first bias is applied to said third line.

94. (Withdrawn) A memory circuit comprising:

a single spin transistor according to claim 86 arranged in a matrix;

a first line connecting each first electrode structure to ground;

a plurality of wordlines commonly connecting said third electrode structures of said spin transistors arranged in the column direction; and

a plurality of bitlines commonly connecting said second electrode structures of said spin transistors arranged in the row direction.

95. (Withdrawn) A memory circuit comprising:

the spin transistor according to claim 86 arranged in a matrix;

a first line connecting each first electrode structure to ground;

a plurality of wordlines commonly connecting said third electrode structures of said spin transistors arranged in the column direction;

a plurality of bitlines commonly connecting said second electrode structures of said spin transistors arranged in the row direction;

an output terminal formed on one end of said bitlines; and

a second line branching from said bitline and connected to a power supply via a load.

96. (Withdrawn) The memory circuit according to claim 94, further comprising a first separate line and a second separate line that intersect one another above said transistor in an electrically insulated manner.

97. (Withdrawn) The memory circuit according to claim 96, wherein said first separate line and/or said second separate line are replaced with said wordline and/or said bitline.

98. (Withdrawn) The memory circuit according to claim 96, wherein information is written by reversing the magnetization of said free layer by a magnetic field induced by causing a current to flow through said wordline and said bitline, thereby changing the relative magnetization configuration between said pin layer and said free layer.

99. (Withdrawn) The memory element according to claim 94, wherein information is sensed using the output characteristics of said spin transistor when a first bias is applied to said wordline and a second bias is applied between said first line and said bitline.

100. (Withdrawn) The memory element according to claim 95, wherein information is sensed using an output voltage that is obtained on the basis of a voltage drop across said load due to a current through said load and said spin transistor between said power supply and said first line when a first bias is applied to said third line.

101. (Withdrawn) A memory element comprising:

a first and a second spin transistor according to claim 86;

a first line connecting the first electrode structure, which is common to said first and said second spin transistors, to ground;

a second and a third line connected to the second electrode structure of said first spin transistor and the second electrode structure of said second spin transistor, respectively; and

a fourth line connected to the third electrode structure of said first spin transistor and the third electrode structure of said second spin transistor.

102. (Withdrawn) A memory circuit comprising:

a plurality of spin transistors according to claim 86 arranged in a matrix;

a first line commonly connecting to ground the first electrode structures of a plurality of spin transistors arranged in a first row and the first electrode structures of a plurality of spin transistors arranged in an adjacent, second row;

a first bitline commonly connecting the second electrode structures of a plurality of spin transistors arranged in a first row and the second electrode structures of a plurality of spin transistors arranged in a second row adjacent to said first row in the column direction;

a second bitline commonly connecting the second electrode structures of said spin transistor in said first row and the second electrode structures of said second spin transistors in said second row adjacent to said first row in the column direction; and

a wordline commonly connecting the third electrode structures of said plurality of spin transistors in a column direction.

103. (Withdrawn) A memory circuit comprising:

a plurality of spin transistors according to claim 86 arranged in a matrix;

a plurality of first lines each commonly connecting to ground said first electrode structures of a plurality of spin transistors in a first row and those of a plurality of spin transistors in a second row adjacent to said first row in the column direction, wherein each of said first lines is provided for every two rows;

a plurality of first bitlines each commonly connecting said second electrode structures of a plurality of said spin transistors arranged in a first row, wherein each of said first bitlines is provided for every two rows;

a plurality of second bitlines each commonly connecting the second electrode structures of a plurality of spin transistors arranged in a second row adjacent said first row in the column direction, wherein one such second bitline is provided for every two rows of said spin transistors; and

a plurality of wordlines commonly connecting the third electrode structures of a plurality of said spin transistors arranged in the column direction.

104. (Withdrawn) The memory element according to claim 90, wherein information is written by reversing the magnetization in said free layer by a magnetic field induced by causing a current to flow through said second line or said third line with which said first separate line or said second separate line have been replaced, or through said first separate line or said second separate line that has not been replaced thereby, thus changing the relative magnetization configuration between said pin layer and said free layer.

105. (Withdrawn) The memory circuit according to claim 97, wherein information is written or rewritten by causing the relative magnetization configuration between said free layer and said pin layer to be changed by a magnetic field induced by causing a current to flow through said wordline or said bitline with which said first separate line or said second separate line have been replaced, or through said first separate line or said second separate line that has not been replaced thereby.

106. (Withdrawn) A transistor comprising:

a spin injector for injecting spin-polarized hot carriers by a spin filter effect; and

a spin analyzer for selecting the thus spin-polarized hot carriers by the spin-filter effect, wherein

at least one of said spin injector and said spin analyzer comprises a barrier layer formed by a ferromagnetic material.

107. (Withdrawn) A transistor comprising:

a spin injector for injecting spin-polarized carriers by a spin filter effect; and

a spin analyzer for selecting the thus spin-polarized carriers by the spin-filter effect, wherein

at least one of said spin injector and said spin analyzer comprises a barrier layer formed by a ferromagnetic material.

108. (Withdrawn) A transistor comprising:

an emitter formed by a ferromagnetic material;

a base formed by a ferromagnetic material;

a collector formed by a nonmagnetic material or a ferromagnetic material;

a first barrier layer comprising a nonmagnetic material disposed between said emitter and said base; and

second barrier layer comprising a nonmagnetic material disposed between said base and said collector, wherein

spin-polarized carriers are injected from said emitter to said base by Fowler-Nordheim tunneling.

109. (Withdrawn) The transistor according to claim 108, wherein said emitter and said base are formed by a ferromagnetic metal or a ferromagnetic semiconductor.

110. (Withdrawn) The transistor according to claim 108, wherein said emitter and said base are formed by a ferromagnetic semiconductor, and said firs and second barrier layers are formed by a semiconductor.

111. (Withdrawn) The transistor according to claim 108, wherein a room temperature operation is enabled by adjusting the barrier height of said first barrier layer and said second barrier layer.

112. (Withdrawn) The transistor according to claim 108, wherein the current transmission rate of the carriers injected from said emitter to said base depends on the relative magnetization directions of said emitter and said base.

113. (Withdrawn) A transistor comprising:

an emitter formed by a ferromagnetic material;

a base formed by a ferromagnetic material;

a collector formed by a nonmagnetic material or a ferromagnetic material;

a first barrier layer disposed between said emitter and said base; and

a second barrier layer disposed between said base and said collector, wherein spin-polarized carriers are injected from said emitter to said base by thermal release.

114. (Withdrawn) The transistor according to claim 113, wherein said emitter and said base are formed by a ferromagnetic metal or a ferromagnetic semiconductor, and said first and second barrier layers are formed by a semiconductor.

115. (Withdrawn) The transistor according to claim 113, wherein said emitter and said first barrier layer are formed using an ohmic contact or a tunnel contact.

116. (Withdrawn) The transistor according to claim 113, wherein a barrier structure between said base and said first barrier layer is formed by a Schottky junction when said base is a ferromagnetic metal, or by a band discontinuity between said base and said first barrier layer when said base is a ferromagnetic semiconductor.

117. (Withdrawn) The transistor according to claim 113, wherein a barrier structure between said base and said second barrier layer is formed by a Schottky junction when said base is a ferromagnetic metal, or by a band discontinuity between said base and said second barrier layer when said base is a ferromagnetic semiconductor.

118. (Withdrawn) The transistor according to claim 113, wherein said emitter is formed by a ferromagnetic semiconductor, said base is formed by a ferromagnetic metal, and said first barrier layer is formed by a Schottky barrier that is formed between a ferromagnetic semiconductor and a ferromagnetic metal.

119. (Withdrawn) The transistor according to claim 113, wherein the current transmission rate of the carriers injected from said emitter to said base depends on the relative magnetization directions of said emitter and said base.

120. (Withdrawn) A transistor comprising:

an emitter formed by a ferromagnetic semiconductor of a first conduction type;

a collector formed by a ferromagnetic semiconductor of a second conduction

type; and

a base formed by a nonmagnetic semiconductor of a second conduction type different from said first conduction type, wherein

the width of said base is adjusted to be such that a tunneling of the carriers from said emitter to said collector can take place.

121. (Withdrawn) The transistor according to claim 120, wherein the emitter-base junction and the base-collector junction are formed by a heterojunction of type II such that said base forms a tunnel barrier with respect to the majority carriers of said emitter and said collector and said emitter and said collector form an energy barrier with respect to the majority carriers of said base.

122. (Withdrawn) The transistor according to claim 120, wherein the magnitude of mutual conductance or output current can be controlled by the relative magnetization directions of said emitter and said collector.

123. (Withdrawn) A transistor comprising:

a ferromagnetic semiconductor layer;

a source and a drain formed with respect to said ferromagnetic semiconductor layer; and

a gate electrode formed with respect to said ferromagnetic semiconductor layer, wherein

at least one of said source and said drain is formed by a ferromagnetic material.

124. (Withdrawn) The transistor according to claim 123, wherein the ferromagnetic material used in at least one of said source and said drain is a ferromagnetic metal or a ferromagnetic semiconductor.

125. (Withdrawn) The transistor according to claim 123, wherein at least one of said source and said drain is formed by a Schottky junction of a ferromagnetic metal and said ferromagnetic semiconductor layer.

126. (Withdrawn) The transistor according to claim 123, comprising a gate insulating layer disposed between said ferromagnetic semiconductor layer and said gate electrode.

127. (Withdrawn) The transistor according to claim 123, wherein the magnitude of mutual conductance or output current can be controlled by the relative magnetization directions of said source or said drain and said ferromagnetic semiconductor material.

128. (Withdrawn) A transistor comprising a tunnel junction structure and a gate electrode, wherein

said tunnel junction structure comprises:

a tunnel barrier formed by an insulating nonmagnetic material;

a source formed by a ferromagnetic material; and

a drain formed by a ferromagnetic material, said tunnel barrier being disposed between said source and said drain, wherein said gate electrode is formed with respect to said tunnel barrier.

129. (Withdrawn) The transistor according to claim 128, wherein the ferromagnetic material used in said source and said drain is said ferromagnetic metal or a ferromagnetic semiconductor.

130. (Withdrawn) The transistor according to claim 128, wherein the thickness of said tunnel barrier is set to be such that a tunnel current can take place from said source to said drain with the application of a voltage to said gate electrode.

131. (Withdrawn) The transistor according to claim 128, wherein the magnitude of mutual conductance or output current can be controlled by the relative magnetization directions of said source and said drain.

132. (Withdrawn) A transistor comprising:

a tunnel junction structure and a gate electrode, wherein

said tunnel junction structure comprises:

a tunnel barrier formed by an insulating nonmagnetic material;

a source formed by a ferromagnetic material; and

a drain formed by a nonmagnetic material or a ferromagnetic material, said

tunnel barrier being disposed between said source and said drain, wherein said gate electrode is formed with respect to said tunnel barrier.

133. (Withdrawn) The transistor according to claim 132, wherein the ferromagnetic material used in said source or said drain is a ferromagnetic metal or a ferromagnetic semiconductor.

134. (Withdrawn) The transistor according to claim 132, wherein the thickness of said tunnel barrier is set to be such that a tunnel current can take place from said source to said drain with the application of a voltage to said gate electrode.

135. (Withdrawn) The transistor according to claim 132, wherein the magnitude of mutual conductance or output current can be controlled by the relative magnetization directions of said source and said tunnel barrier.

136. (Withdrawn) A memory element comprising:

one transistor according to claim 106;

an information rewriting means for rewriting information in said transistor by causing the magnetization state of a ferromagnetic material contained in said transistor; and

an information reading means for reading the information stored in the form of a magnetization state, from the output characteristics of said transistor.

137. (Withdrawn) The memory element according to claim 135, wherein the transistor comprising a spin injector for injecting spin-polarized hot carriers by a spin filter effect; and a spin analyzer for selecting the thus spin-polarized hot carriers by the spin-filter effect, wherein at least one of said spin injector and said spin analyzer comprises a barrier layer formed by a ferromagnetic material further comprises a free layer having a ferromagnetic material in which the direction of magnetization can be independently controlled, and a pin layer having a ferromagnetic material in which the magnetization direction is not changed, wherein

a first state in which said free layer and said pin layer have the same magnetization direction, and a second state in which they have different directions of magnetization can be retained.

138. (Withdrawn) A memory element comprising one transistor according to claim 106, wherein information can be stored based on the magnetization direction of said free layer relative to that of said pin layer, and the information stored in said transistor can be detected based on the output characteristics of the transistor that depend on the relative magnetization directions of said pin layer and said free layer.

139. (Withdrawn) A memory element comprising:
one transistor according to claim 108;
a first line connected to said emitter;
a second line connected to said base; and
a third line connected to said collector.

140. (Withdrawn) A memory element comprising:
one transistor according to claim 123;
a first line connected to said source;
a second line connected to said gate; and
a third line connected to said drain.